PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H04B 1/38

A1

(11) International Publication Number: WO 00/69084

(43) International Publication Date: 16 November 2000 (16.11.00)

(21) International Application Number: PCT/US00/12473

(22) International Filing Date: 5 May 2000 (05.05.00)

(30) Priority Data:

60/133,129	7 May 1999 (07.05.99)	US
60/133,135	7 May 1999 (07.05.99)	US
60/133,137	7 May 1999 (07.05.99)	US
60/133,141	7 May 1999 (07.05.99)	US

(71) Applicant: MORPHICS TECHNOLOGY INC. [US/US]; 1550 S. Bascom Avenue, Campbell, CA 95008-0638 (US).

(72) Inventor: SUBRAMANIAN, Ravi; 150 Alley Way, Mountain View, CA 94040 (US).

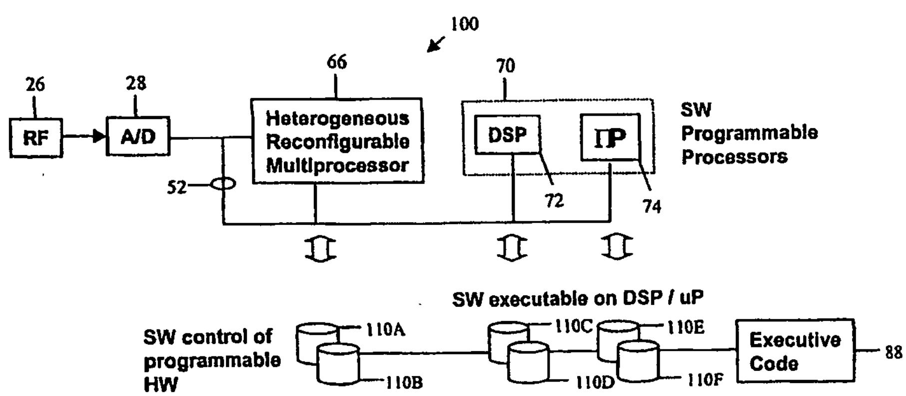
(74) Agents: GALLIANI, William, S. et al.; Pennie & Edmonds LLP, 1155 Avenue of the Americas, New York, NY 10036 (US).

(81) Designated States: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published

With international search report.

(54) Title: REPROGRAMMABLE DIGITAL WIRELESS COMMUNICATION DEVICE AND METHOD OF OPERATING SAME



(57) Abstract

A digital wireless communication device (100) comprises a software-programmable processor (70), a heterogeneous reconfigurable multiprocessing logic circuit (66), and a bus (52) connecting the software-programmable processor (70) and the heterogeneous reconfigurable multiprocessing logic circuit (66). The heterogeneous reconfigurable multiprocessing logic circuit (66) comprises a set of heterogeneous signal processing kernels and a reconfigurable data router interconnecting the heterogeneous signal processing kernels. The software-programmable processor (70) is selected from a group comprising: a digital signal processor (72) and a central processing unit (74). The architecture provides the ability to reconfigure a single product platform for multiple standards, applications, services, and quality-of service, instead of developing multiple hardware platforms to establish the same collective functionality. The architecture also provides the ability to use software programming techniques to reduce product development time and achieve rapid and comprehensive product customization. The invention extends the performance efficiency of microprocessors and digital signal processors via the augmentation of data path and control paths through a reconfigurable co-processing machine. The reconfigurability of the data path optimizes the performance of the data flow in the algorithms implemented on the processor.

REPROGRAMMABLE DIGITAL WIRELESS COMMUNICATION DEVICE AND METHOD OF OPERATING SAME

This application claims priority to the provisional patent applications with the following Serial Numbers: 60/133,141; 60/133.137; 60/133.129: and 60/133,135, each of which was filed on May 7, 1999.

BRIEF DESCRIPTION OF THE INVENTION

This invention relates generally to wireless communication devices. More particularly, this invention relates to a reconfigurable digital wireless communication device.

BACKGROUND OF THE INVENTION

Existing communication devices are "static" devices. That is, they are designed to support a specific wireless communication standard and/or to support a specific application (e.g., voice, data transmission) at a specific data rate. Typically, different wireless communication standards are used in different wireless networks, both within a geographic locality and worldwide. Thus, an individual traveling between different regions is required to use a separate wireless communication device in each region.

In addition, the advent of new and evolving user applications and services may necessitate redesign of static wireless communication infrastructure and terminals. Thus, an individual or service provider who wants to utilize or enable such services is required to replace or upgrade equipment.

dataflow into and out of the programmable logic device 62. The software-programmable processors 70 typically comprises a digital signal processor 72 and a control microprocessor 74. For lower bandwidth applications (tens of kbps), software-programmable digital signal processors 72 are typically used to perform requisite signal processing functions. For high bandwidth applications (tens of Mbps), a fully hardwired approach is typically employed. The general purpose microprocessor 74 typically performs control and other functions. Accordingly, the signal processing device 50 can be highly optimized only for a particular communication standard, service and application. Prior art approaches to accommodating multiple standards, services and applications have essentially consisted of combining the disparate hardware and software resources separately optimized for each service of interest. This results in poor efficiency in terms of size, weight and power consumption.

Figure 2B illustrates the control architecture 80 for a prior art multi-standard communication apparatus. The architecture 80 includes executive code 88, which is effectively an operating system running on microprocessor 74 or digital signal processor 72. One of a suite of applications 84 is selected to run under the operating system. Each application 84 executes a set of software/hardware functions 82A-C. Each application 84 requires computation resources, which are available according to Figure 2A, either via a microprocessor, a digital signal processor, a fixed-function logic engine, or a programmable logic engine. Thus, each of the applications requires some combination of these resources; the actual partitioning among their use is determined by the product/application requirements. For example, operation on a portable device favors much of the functionality being implemented on dedicated, fixed-function hardwired logic devices. On the other hand, product flexibility and upgrade-ability requires use of completely programmable components in the platform, such as microprocessors, digital signal processors, and programmable logic. The approach of Figure 2B is also inefficient, as it essentially relies upon sequentially selecting one of the sets of disparate and redundant hardware and software resources discussed in connection with Figure 2A.

The poor efficiency of the prior art approaches discussed is evident from Figure 3, which depicts energy efficiency vs. flexibility for the various architectural elements of device 50. The highly efficient fixed-hardware resources are highly

The invention provides a communication apparatus that can operate over a plurality of telecommunication physical layer standards, radio frequency bands, data-rates, and user-programmed or network-programmed services. The functionality of a device constructed in accordance with the invention is defined as a set of software modules, each including a combination of "personalities" for the hardware devices of the apparatus. The software modules comprise object code that executes on a microprocessor, a digital signal processor, or on a heterogeneous reconfigurable multiprocessing logic module. The invention enables the use of a single hardware platform to operate over a variety of bands, standards, and data rates, while delivering a variety of user-programmed or network-programmed services. Furthermore, the invention can be reconfigured in the factory or field through various means including but not limited to factory/point-of-sale programming, remote control, and over-the-air or over-the-network download.

Thus, the invention significantly reduces the number of product platforms required to span a large product offering space for the wired or wireless communication market.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the invention, reference should be made to the following detailed description taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a digital communication modem that may be implemented in accordance with the prior art.

FIGURE 2A illustrates an architecture used to implement a prior art digital communication modem.

FIGURE 2B illustrates a control strategy used to implement a prior art digital communication modem.

FIGURE 3 illustrates the Energy-flexibility Gap associated with the prior art.

FIGURE 4A illustrates a reconfigurable digital wireless communication device in accordance with an embodiment of the invention.

DSP microprocessor 72 and control microprocessor 74. The new architecture exploits heterogeneous reconfigurable multiprocessor 66, which includes a pool of parallel heterogeneous hardware signal processors referred to as signal processing kernels. The kernels perform the more computationally intensive signal processing operations of a set of standards, applications and services of interest, and are selected and configured in a modular, non-redundant manner. The individual signal processing kernels and their interconnections can be quickly reconfigured, so that device 100 can quickly switch from one standard, application, and/or service of interest to another. DSP 72 performs the less computationally intensive signal processing functions, while microprocessor 74 performs control and other functions. A communication bus 52 links microprocessor 74, digital signal processor 72, and heterogeneous reconfigurable multiprocessing hardware 66. Each hardware device is controlled by a corresponding software module 110.

The communication apparatus of the invention can change its function temporally via a mechanism that is under software control. Figure 4B illustrates the executive code 88 and software modules 110 of the invention operating in connection with the hardware platform 100 of Figure 4A. As shown in Figures 4A-B, selected software modules 110 execute on different hardware components. Thus, for example, software kernels 110A-B are executed on heterogeneous reconfigurable multiprocessing hardware 66, software kernels 110C-D are executed on the digital signal processor 72, and software kernels 110E-F are executed on the microprocessor 74. Executive code 88 further facilitates the management of the dataflow into and out of heterogeneous reconfigurable multiprocessor 66, as well as the functionality of heterogeneous reconfigurable multiprocessor 66. Thus, all the dataflow and control flow of all computational resources may be controlled and reconfigured via a software-programmable engine.

The software modules 110 define a superset of signal processing and control functions required by the suite of standards, applications, and/or services of interest, in accordance with the matrix of Figure 4B. In one embodiment, the software modules 110 are platform-dependent, and are thus in the form of object code optimized for the platform under consideration. They reside either in the product platform memory or are downloadable over-the-network, over-the-air, on the manufacturing floor, or point-

including: power efficiency. memory requirements. throughput. latency, and flexibility. Function mapping will also rely upon product application space. multi-nation. multi-standard. or multi-service product operation requirements, product development time. and time-to-market requirements. Thus, the same hardware can be programmed and/or reconfigured to implement the same dataflow and control flow, but with a new set of parameters. that may be product quality-, channel-, standard-, service-, or country-of-operation-dependent.

An example mapping of the Digital Front End Processor, Detector / Demodulator and Parameter Estimator of Figure 1 onto the architecture of Figure 4A is given in Figure 6. This figure illustrates a digital communication modem 140 that may be implemented in accordance with an embodiment of the invention. A transmitter transmits a signal to a channel, which may be a wireless or physical channel. The transmitted signal is received at the modem 140, where it is initially processed by a Radio Frequency (RF) subsystem 26. The RF subsystem 26 performs analog mixing, analog filtering, and analog gain control functions. The analog signal from the RF subsystem 26 is then converted to an equivalent digital signal with the analog-to-digital converter 28.

The output from the RF subsystem 26 is one or more bandpass signals (intermediate frequency signals), which are then digitized by the analog-to-digital converter 28, which is typically implemented as a free-running analog-to-digital converter. The output from the analog-to-digital converter 28 is placed on a bus 55, which may be reconfigurable. Signals from the bus 55 are routed to the hardware-reconfigurable digital front-end processor 142. Preferably, the reconfigurable processor 142 is implemented with a heterogeneous reconfigurable multiprocessor as discussed above.

The reconfigurable digital front-end processor 142 performs channel selection, sample-rate conversion, digital down-conversion, and digital filtering. This is achieved through the use of multi-rate digital signal processing techniques, software-programmable filter coefficients, rate-conversion, channelization, and loop filter parameters. The output of reconfigurable processor 142 consists of complex IQ signals, which are then fed to a demodulation-detection-parameter estimation processor 144. The functionality of processor 144 is distributed between the software-

reconfigurable multiprocessor 160 is comprised of a set of heterogeneous data processing kernels 162 and a reconfigurable data router 168. The configuration of the heterogeneous data processing kernels 162 is determined by control bus 152, while the configuration of data router 168 is determined by control bus 154.

The data flow and control flow computation kernels 162 are of varying granularity, from simple arithmetic operators, such as adders and multipliers, to more complex data flow/control flow operations, such as a complete Viterbi Algorithm Add-Compare Select and Fast Fourier Transform Butterfly units. The composition of computation kernels 162 is further discussed below.

Figure 8 illustrates architecture 150 in greater detail. The PCU 151 receives a module of executive code 88 from microprocessor 74 of Figure 6. The executive code is a segment of the microprocessor executable programs stored in memory that orchestrates overall configuration and functionality. A controller 156 configures a set of quasi-fixed-function logic kernels 162A-C. In a typical application, the executive code 88 executes on the control microprocessor 74 or DSP microprocessor 72, and the functionality of controller 156 is allocated to the microprocessors and associated peripherals such as memory and various bus interfaces. Figure 8 further illustrates that individual kernels may be interconnected either directly, as per representative path 164, or via reconfigurable data router 168. Reconfigurable data router 168 further receives input data from and delivers output data to bus 55. Reconfigurable data router 168 is controlled by the data router manager 158 via control bus 154, and in turn via controller 156 and executive code 88 of Figure 4A.

The portfolio of kernels 162 is determined by first profiling the applications of interest, as discussed below. Kernels 162 are compute engines, and their nature as well as that of their interconnection is governed by any bit-slice, nibble-slice, and word-slice routing control mechanism, including, but not limited to, a programmable bus. A preferred canonical architecture for the kernels 162 is depicted in Figure 9A. A configurable arithmetic logic unit (ALU) 186 performs the necessary signal processing operations. A local memory 182 serves as a high-speed cache. Data Sequencer 184 orchestrates the flow of data between local memory 182 and ALU 186. For further illustration, Figure 9B shows several representative or available configurable architectures that may be implemented by one or more kernels 162.

the hardware reconfigurable processor 142. functions 204 B-E to be provided by coprocessor 146. and corresponding MOPS required by each function 204. These metrics are calculated for the various pertinent signal processing datapaths.

Additionally in this step, computationally intensive functions are further categorized according to type of operation. e.g., arithmetic/logical. control. and memory access. For each category. characteristic power per MOPS is determined for hardware or software implementation from vendor data. analysis. or other means. Power. e.g., milliwatts. required per function is thereby characterized for implementation in both reconfigurable hardware or in software (i.e.. running on a processor whose power-per-MOPS has been characterized). In addition. the corresponding code size (and therefore memory requirement) for software implementation is determined. From the above. and from budgeted power and memory resources. allocation of processing operations to hardware and software processors can be determined.

The entries in spreadsheet 200 correspond to static operation for a particular standard. i.e.. to a specific time within a dynamic operational scenario. The analysis of Figure 10 must be repeated as necessary to reflect important temporal variations during representative/ realistic scenarios for all standards, applications. and/or services of interest. The results of these analyses must be interpreted to reveal additional critical metrics of computational intensity. including for example but not restricted to average and peak MOPS for each relevant operation. This enables the requisite specifications for the hardware and software processing resources to be further evaluated.

The second step of profiling involves analysis of commonality of signal processing functions across the standards. applications. and/or services of interest. This is represented by example in Figure 11. Included in abridged spreadsheet 220 are representative standards/ applications. and respective relevant signal processing functions within the general category of parameter estimation. Figure 11 shows. for example. that a Windowed Average Energy Estimator is required by seven of the listed standards. The designer would research the respective requirements of each of these seven standards to determine the required superset and seven subsets of functionality.

kernel pool 280 includes a sufficient number of each type of kernel to permit the assembly of multiple datapaths 290. In turn. a sufficient multiplicity of datapaths 290 is assembled to accommodate the signal processing requirements of a particular standard. service or application. This is illustrated for a number of representative applications and/or products 300. The portfolio 300A-D can represent either a single product having multi-mode/standard /application capability. or multiple. separate products based on common underlying hardware and software resources.

Thus. a manufacturer can enjoy mass customization based on a common product "platform." Initial or subsequent configuration can be performed in the factory. at point-of-sale. or by the user after delivery. Post-delivery customization can be based upon any of a number of techniques. including but not limited to smart card, wired interface. and over-the-air/over-the-network download and billing.

In Figure 14. the various kernels 162 are interconnected by the reconfigurable data router 168 of Figures 7-8. For simplicity. however. reconfigurable data router 168 is not shown in Figure 14.

For convenience. the above discussion has utilized examples relating to wireless communication systems. The principles discussed apply directly to other applications including but not limited to multimedia. security. and networking. Furthermore. the receive path only has been illustrated; the apparatus and method of the invention apply directly to the transmit path.

Those skilled in the art will recognize a number of benefits associated with the disclosed architecture. The architecture provides the ability to reconfigure a single product platform for multiple standards. applications. services. and quality-of service, instead of developing multiple hardware platforms to establish the same collective functionality. The architecture also provides the ability to use software programming techniques to reduce product development time and achieve rapid and comprehensive product customization. Thus. new services can be provided via software upgrades. The apparatus of the invention allows a network operator or service provider to control a communication terminal's capabilities. Equipment manufacturers may exploit the invention to create software-defined communication appliances.

Advantageously. the architecture of the invention optimally combines fixed-function and reconfigurable logic resources. The system has reconfigurable control

teachings. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications. the thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims and their equivalents.

selecting a set of parameters and values required to implement a specified wireless communication application. standard. and service;

downloading said set of parameters and values to a digital wireless communication device including a heterogeneous reconfigurable multiprocessing logic circuit with a plurality of re-programmable data processing kernels: and

operating said plurality of re-programmable data processing kernels in accordance with said set of parameters and values to support said specified communication application. standard. and service.

7. The method of claim 6 wherein said selecting step includes the step of selecting a set of parameters and values from the group comprising: a country of operation. a frequency band. and a data rate.

8. The method of claim 6 wherein said downloading step includes the step of downloading said set of parameters over a wireless communication channel.

9. The method of claim 6 wherein said downloading step includes the step of downloading said set of parameters at the time of manufacture.

10. The method of claim 6 wherein said downloading step includes the step of downloading said set of parameters at a point of sale.

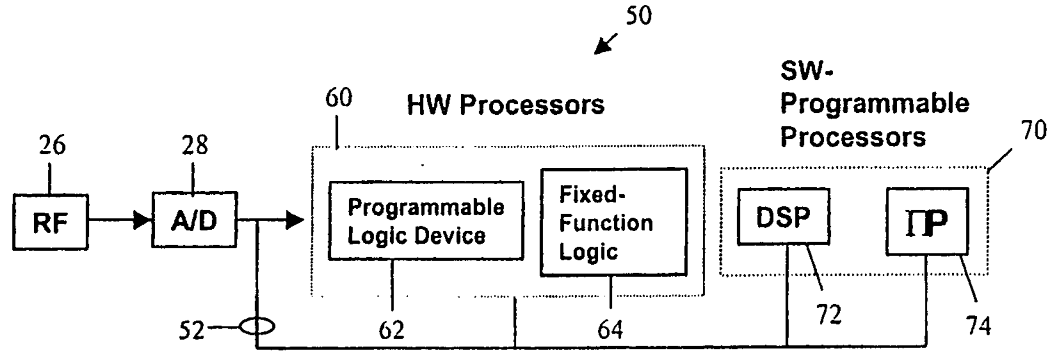


Fig. 2A (Prior Art)

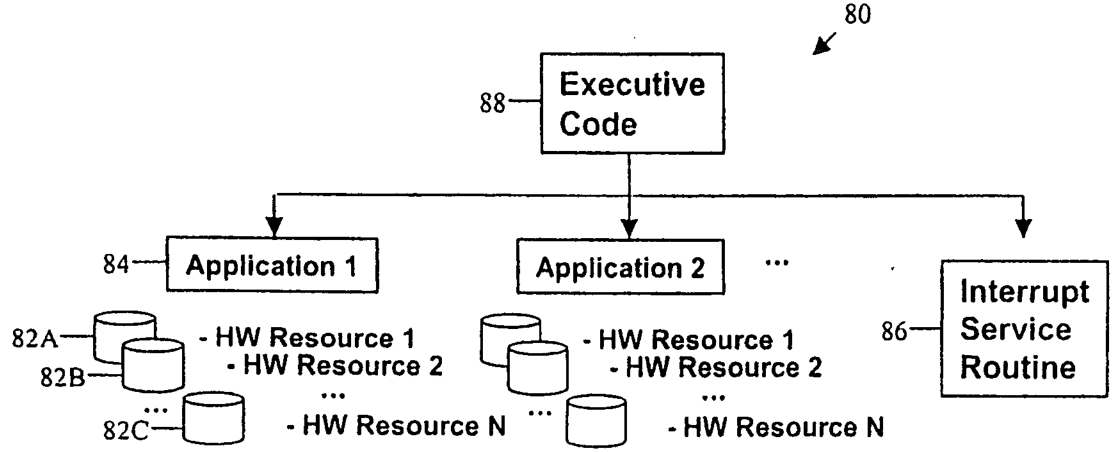


Fig. 2B (Prior Art)

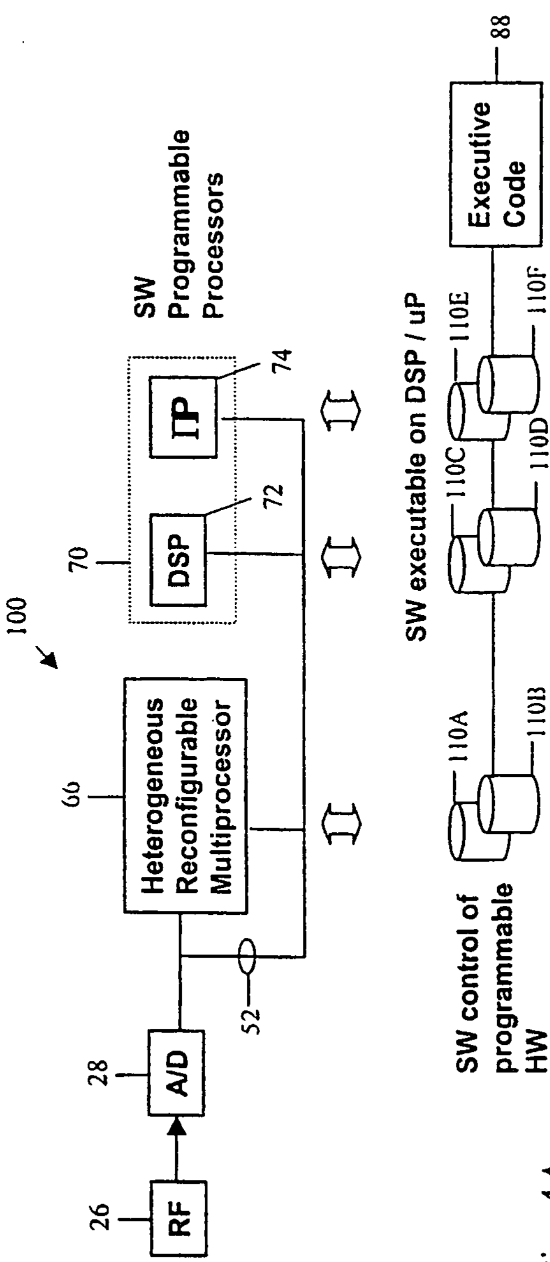

100
RF
26
A/D
28
52
Heterogeneous Reconfigurable Multiprocessor
66
70
DSP
72
μP
74
SW Programmable Processors
SW control of programmable HW
SW executable on DSP / uP
110A
110B
110C
110D
110E
110F
Executive Code
88

Fig. 4A

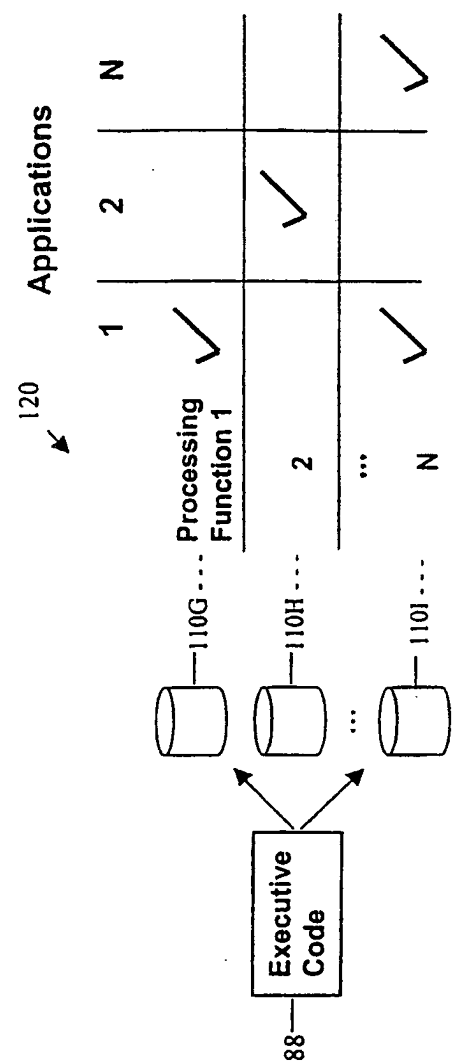

120
Applications
1
2
N
Processing Function 1
2
...
N
110G - - -
110H - - -
110I - - -
Executive Code
88

Fig. 4B

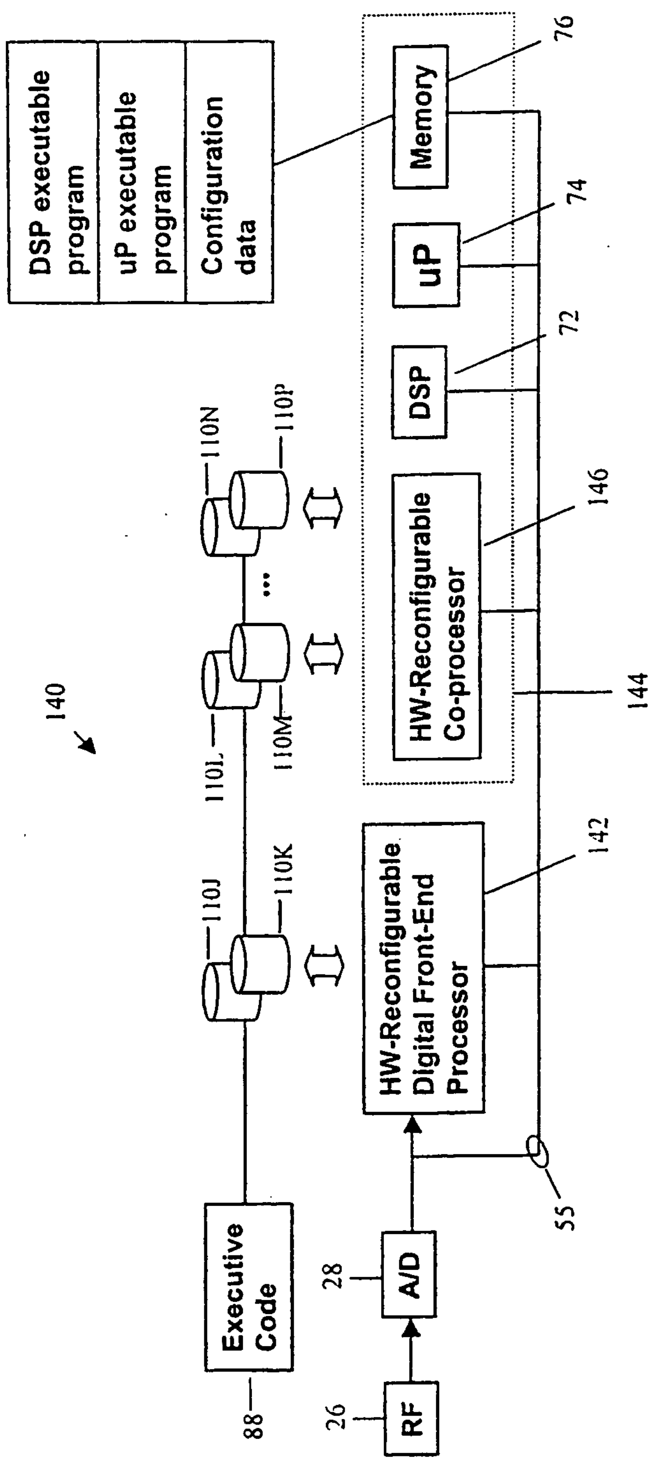

DSP executable program
uP executable program
Configuration data
76
Memory
74
uP
72
DSP
110N
110P
146
HW-Reconfigurable Co-processor
140
110L
110M
144
110J
110K
142
HW-Reconfigurable Digital Front-End Processor
Executive Code
88
A/D
28
RF
26
55

Fig. 6

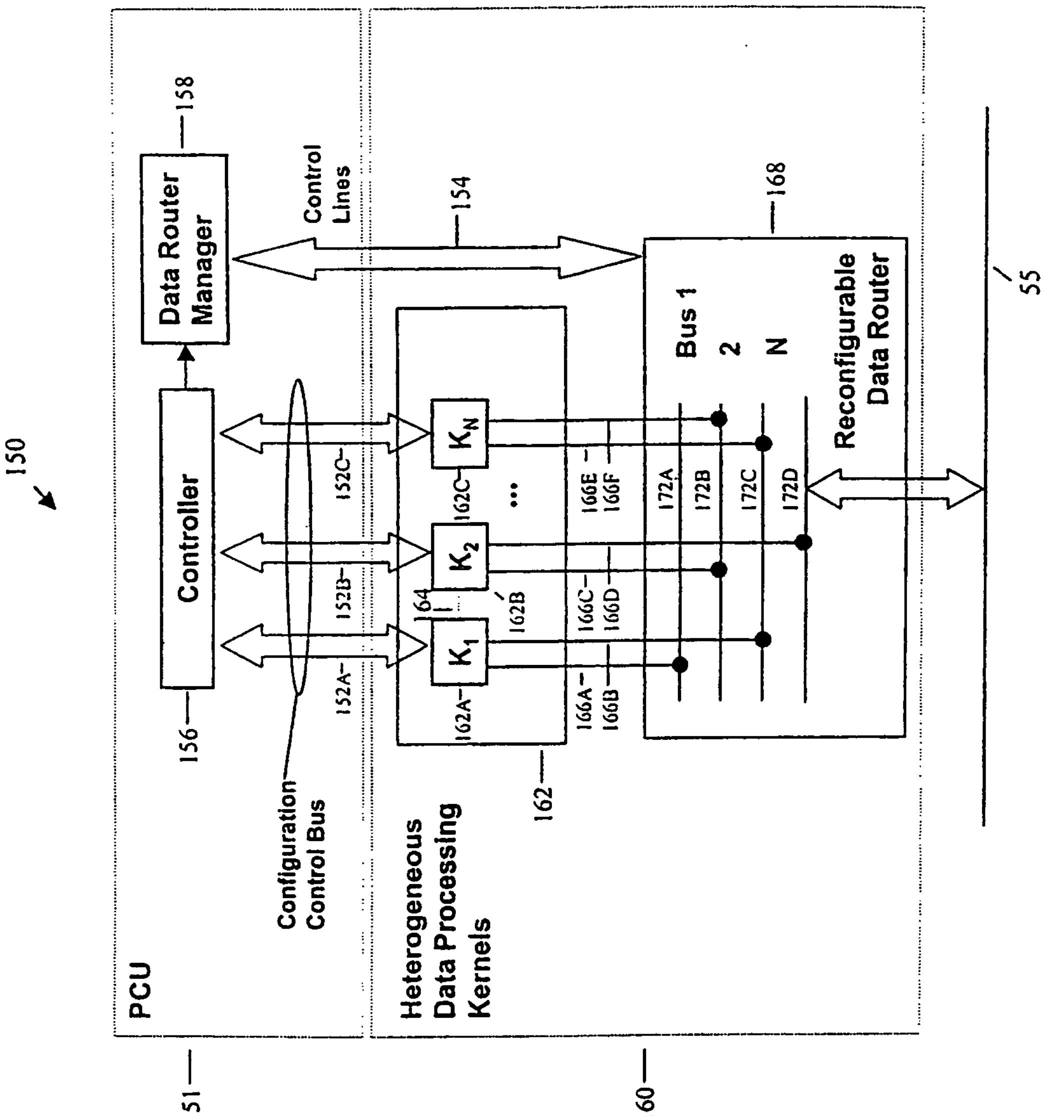

150
PCU
151
Controller
156
Data Router Manager
158
Control Lines
154
Configuration Control Bus
152A
152B
152C
Heterogeneous Data Processing Kernels
160
162
K_1
K_2
K_N
162A
162B
162C
164
166A
166B
166C
166D
166E
166F
Bus 1
2
N
172A
172B
172C
172D
168
Reconfigurable Data Router
55

Fig. 8

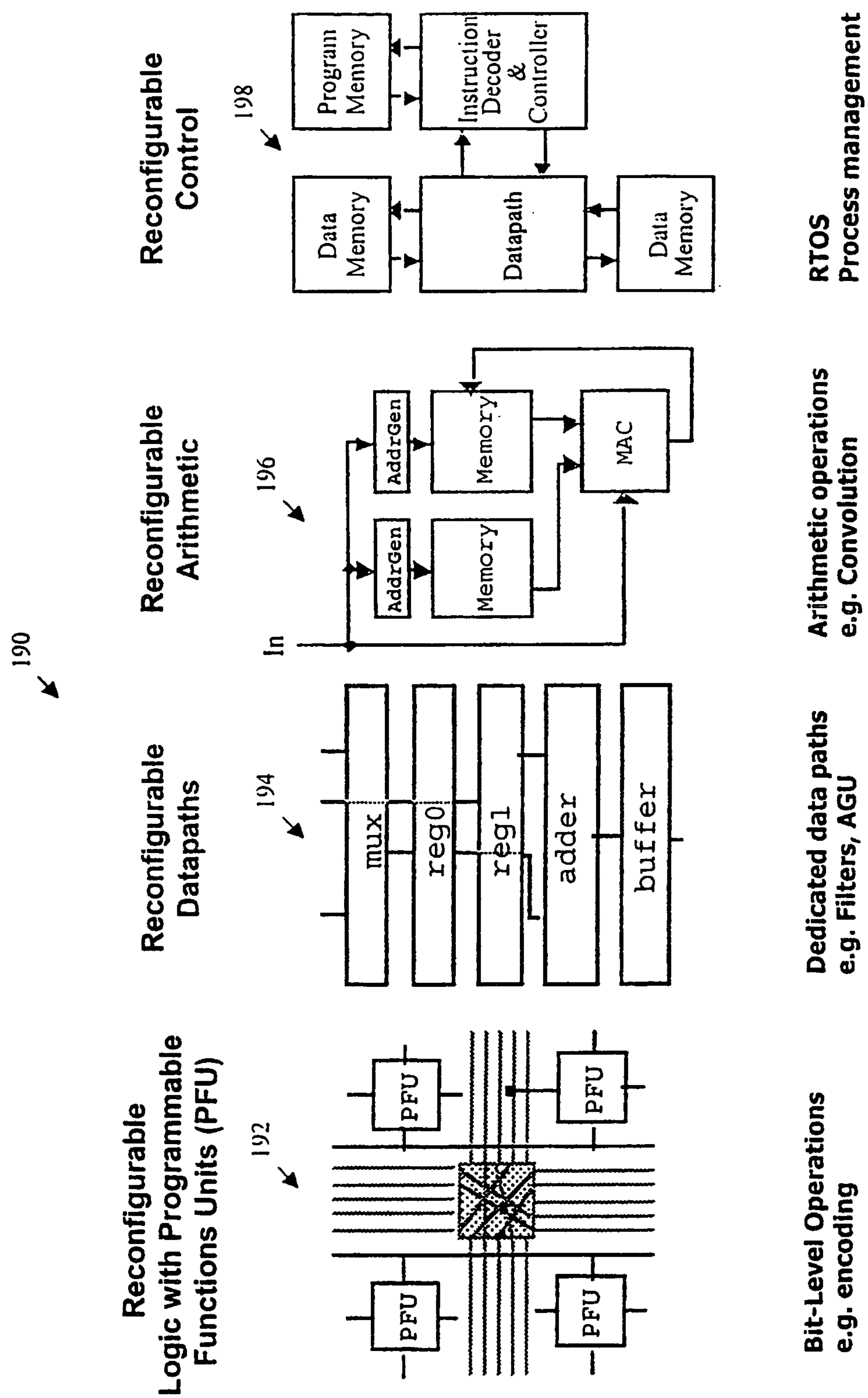

190
Reconfigurable
Logic with Programmable
Functions Units (PFU)
192
PFU
PFU
PFU
PFU
Bit-Level Operations
e.g. encoding
Reconfigurable
Datapaths
194
mux
reg0
reg1
adder
buffer
Dedicated data paths
e.g. Filters, AGU
Reconfigurable
Arithmetic
196
In
AddrGen
AddrGen
Memory
Memory
MAC
Arithmetic operations
e.g. Convolution
Reconfigurable
Control
198
Program
Memory
Instruction
Decoder
&
Controller
Data
Memory
Datapath
Data
Memory
RTOS
Process management

Fig. 9B

220

	TDMA				CDMA				
	IS136	GSM	GPRS	EDGE	IS-95B	IS-2000	WCDMA-FDD	GPS	Globalstar
Parameter Estimation Functions									
LMS Channel Estimator		x	x	x					
Windowed Average Energy Estimator	x	x	x	x	x	x	x		
ML Symbol Timing Estimator	x	x	x	x	x	x	x	x	x
ML Carrier Phase Estimator	x	x	x	x	x	x	x	x	x
PN Correlator					x	x	x		
MatchedFilter							x	x	x
Interference Energy Estimator						x	x		

Fig. 11

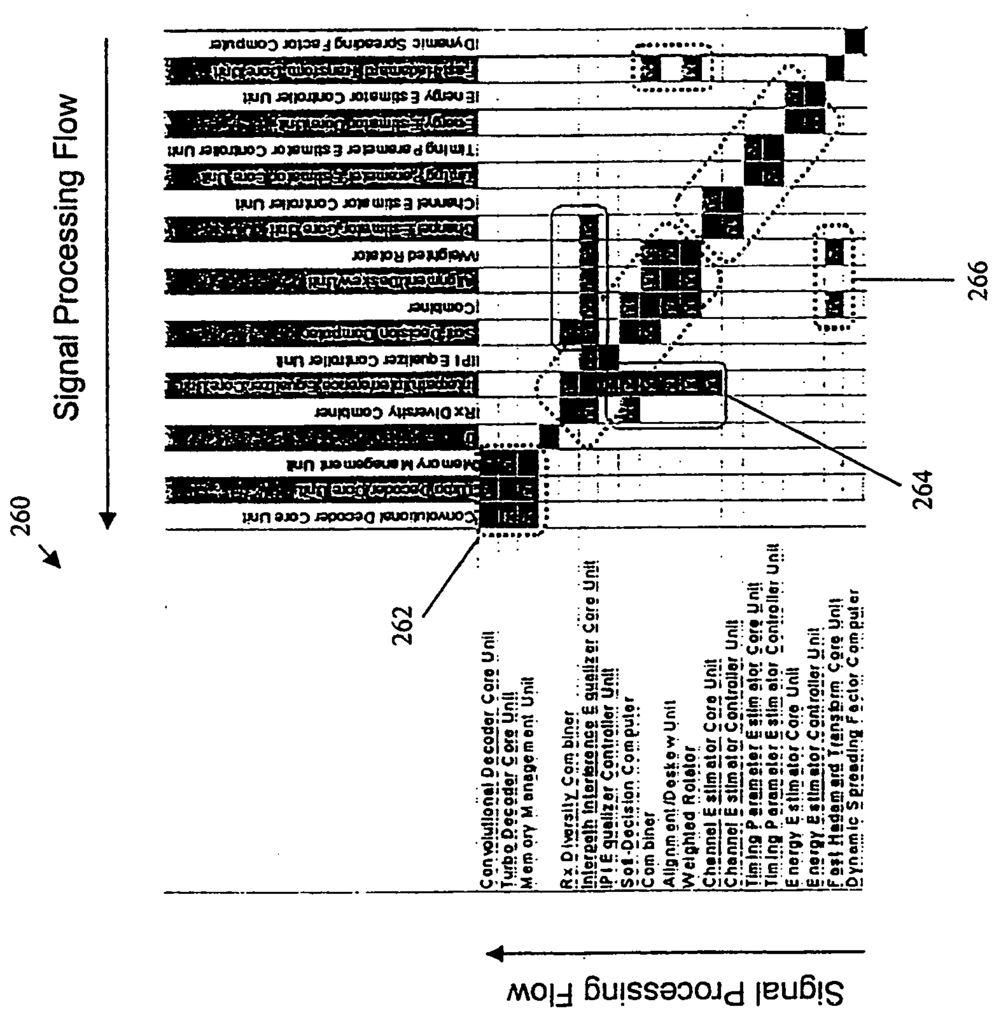

Signal Processing Flow
260
262
264
266
Convolutional Decoder Core Unit
Turbo Decoder Core Unit
Memory Management Unit
Rx Diversity Combiner
Interpath Interference Equalizer Core Unit
IPI Equalizer Controller Unit
Soft-Decision Computer
Combiner
Alignment/Deskew Unit
Weighted Rotator
Channel Estimator Core Unit
Channel Estimator Controller Unit
Timing Parameter Estimator Core Unit
Timing Parameter Estimator Controller Unit
Energy Estimator Core Unit
Energy Estimator Controller Unit
Fast Hadamard Transform Core Unit
Dynamic Spreading Factor Computer
Signal Processing Flow

Fig. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/12473

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H04B 1/38
US CL :375/219
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/219, 220, 222, 295, 316

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST (wireless communication, programmable wireless communication, ADC, programmable processor, PLA, PAL, logic arrays, multiprocessors)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,872,810 A (PHILIPS et al.) 16 FEBRUARY 1999, abstract, and figures 1, 7, 8, and 17-21	1-10
Y	US 5,539,479 A (BERTRAM) 23 JULY 1996, figures 3, 5, 9-12 and col. 1, line 31 to col.2, line 42.	1-10

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search 27 JULY 2000	Date of mailing of the international search report 15 AUG 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer MOHAMMAD Jamoun R. Matthews Telephone No. (703) 306-3034

Form PCT/ISA/210 (second sheet) (July 1998)★